IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: Bu et al. | Docket No.: TI-36637

Serial No.: 10/810,905 | Art Unit: 2823

Filed: 03/26/2004 | Examiner: Stark, J. J.

Confirmation No.: 9390

Title: Improved CMOS Transistors and Methods of Forming Same

APPELLANTS' BRIEF

July 29, 2008

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

In response to the final Office Action, dated 04/30/2008, the Appellants submit this Appellants' Brief. The Commissioner is hereby requested and authorized to charge any required fees for the filing of this document to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

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REAL PARTY IN INTEREST

The Real Party in Interest in the present appeal is Texas Instruments Incorporated, the assignee, as evidenced by the assignment set forth at Reel 015157, Frame 0279.

RELATED APPEALS AND INTERFERENCES

The divisional case is currently under appeal and its status is "Appeal Ready for Review" in Private PAIR. The application number of this divisional case is 11/372,430 and it was filed 03-09-2006. The appeal number is unknown. Jarrett J. Stark is the Examiner for the present application and the divisional application.

STATUS OF CLAIMS

Claims 1-10 and 19-20 are the subject of this appeal. Claims 1-20 are pending, Claims 1-10 and 19-20 are rejected, and Claims 11-18 are withdrawn from consideration.

STATUS OF AMENDMENTS

The Appellants filed an amendment, dated June 5, 2006, in response to the non-final Office Action dated March 28, 2006. The Appellants filed an amendment, dated September 13, 2006, in response to the final Office Action dated July 12, 2006.

The Appellants filed a Request for Continued Examination on October 9, 2006 in response to the Advisory Action dated September 28, 2006.

The Appellants filed an amendment, dated January 30, 2007, in response to the non-final Office Action dated October 31, 2006. The Appellants filed an amendment, dated June 28, 2007, in response to the non-final Office Action dated April 3, 2007. The Appellants filed an amendment, dated September 8, 2007, in response to the final Office Action dated August 8, 2007.

The Appellants filed a Request for Continued Examination on October 4, 2007 in response to the Advisory Action dated September 21, 2007.

The Appellants filed an amendment, dated February 26, 2008, in response to the non-final Office Action dated December 31, 2007. The Appellants file this Appeal Brief in response to the final Office Action dated April 30, 2008.

SUMMARY OF THE CLAIMED SUBJECT MATTER

Independent Claim 1 is directed to a method for fabricating a CMOS transistor structure (FIGS. 2a-2d; page 3 line 4 through page 10 line 20). The method includes providing a semiconductor substrate (element 10 of FIGS. 2a-2d; page 4 lines 21-23 (paragraph 0015)) having an P-type dopant region to support an N-channel transistor of the CMOS transistor structure (page 4 line 25 through page 5 line 2 (paragraph 0015)) and a N-type dopant region to support a P-channel transistor of the CMOS transistor structure (page 4 line 25 through page 5 line 2 (paragraph 0015)), each of the N-type dopant and P-type dopant regions having an overlying gate stack (page 5 lines 4-15 (paragraph 0016)) including a conductive gate structure (element 30 of FIGS. 2a-2d; page 5 lines 4-15 (paragraph 0016)) and a dielectric gate structure (element 20 of FIGS. 2a-2d; page 5 lines 4-15 (paragraph 0016)). The method also includes forming lightly-doped extension regions in the semiconductor substrate adjacent each gate stack (element 100 of FIGS. 2b-2d, page 5 line 17 through page 6 line 11 (paragraphs 0017-0019)), forming a layer of insulating material (element 110 of FIGS. 2c-2d; page 6 line 12 through page 7 line 16 (paragraphs 0020-0024)) in contact with a total exposed surface of the lightly-doped extension regions (FIGS. 2c-2d; page 6 line 12 through page 7 line 16, page 9 lines 21-28 (paragraphs 0020-0024 and 0033)), and forming an interfacial layer of nitrogen (element 112 of FIGS. 2c-2d; page 6 line 12 through page 7 line 16, page 9 lines 7-20

(paragraphs 0020-0024, 0032)) within the total exposed surface of the lighted-doped extension regions (page 6 lines 12-29, page 9 lines 7-20 (paragraphs 0020-0021,0032)). In addition, the method includes forming at least one sidewall layer coupled to the layer of insulating material (page 6 lines 12-20, page 7 line 17 through page 8 line 5 (paragraphs 0020 and 0025-0026)), and forming source and drain regions (element 140 of FIG. 2d; page 8 lines 5-11 (paragraph 0027)) in the semiconductor substrate adjacent to each of the gate stacks. Furthermore, the method includes forming a capping layer (element 132 of FIG. 2d; page 8 line 11 through page 9 line 20 (paragraphs 0028-0032)) of contiguous silicon nitride over the semiconductor substrate (page 8 lines 11-18 (paragraph 0028)). Moreover, the method includes annealing (page 8 lines 18 through page 9 line 20 (paragraphs 0029-0032)), after the formation of the capping layer and with the capping layer in place (page 8 lines 18 through page 9 line 20 (paragraphs 0029-0032)), the extension regions and the source and drain regions (page 8 lines 18 through page 9 line 20 (paragraphs 0029-0032)), and removing all of the capping layer after the annealing (page 8 lines 23-28 (paragraph 0030)).

Claim 2 is dependant on Claim 1 and further specifies that the extension regions for the PMOS transistors have a dopant concentration in the range of about 1-2 e20 atoms/cm3 (page 11 lines 28-29, original Claim 2).

Claim 3 is dependant on Claim 1 and further specifies that the source and drain regions for the PMOS transistors have a dopant concentration in the range of about 1-2 e20 atoms/cm3 (page 12 lines 1-2, original Claim 3).

Claim 4 is dependant on Claim 1 and further specifies that the interfacial nitride layer has an atomic nitrogen concentration in the range of 2-15 atomic percent (page 6 lines 11-20 (paragraph 0020)).

Claim 5 is dependant on Claim 1 and further specifies that the insulating layer is selected from the group comprising silicon nitride and silicon oxide (page 6 lines 11-20, page 7 lines 16-28 (paragraphs 0020, 0025)).

Claim 6 is dependant on Claim 1 and further specifies that the step of forming an interfacial layer of nitrogen is performed using one of the methods selected from the group comprising an NH_3 thermal annealing (page 6 lines 20-29 (paragraph 0021)), an NH_3 or N_2 plasma treatment (page 7 lines 12-16 (paragraph 0024)), or an N implantation (page 7 lines 12-16 (paragraph 0024)).

Claim 7 is dependant on Claim 1 and further specifies that the capping layer has a thickness in the range of 200-1000 angstroms (page 8 lines 11-18 (paragraph 0028)).

Claim 8 is dependant on Claim 1 and further specifies that the annealing step is performed in the range of 1000-1100 degrees centigrade for a time in the range of less than about 10 seconds (page 8 lines 18-23 (paragraph 0029)).

Claim 9 is dependant on Claim 1 and further specifies that the gate stack further includes a nitride sidewall deposited with BTBAS precursor (page 7 lines 16-28 (paragraph 0025)).

Independent Claim 10 is directed to a method of fabricating a CMOS structure (FIG. 2d; page 3 line 28 through page 4 line 10, page 4 line 18 through page 10 line 20 (paragraphs 0011 and 0014-0037)). The method includes providing a semiconductor substrate (element 10 of FIGS. 2a-2d; page 4 line 21 through page 5 line 3 (paragraph 0015)) having an N-type dopant region to support a PMOS transistor of the CMOS transistor structure (page 4 line 21 through page 5 line 3 (paragraph 0015)) and a P-type dopant region to support an NMOS transistor of the CMOS transistor structure (page 4 line 21 through page 5 line 3 (paragraph 0015)), each of the N-type dopant and P-type dopant regions having an overlying gate stack (page 5 lines 3-16 (paragraph 0016)) including a conductive gate structure (element 30 of FIGS. 2a-2d; page 5 lines 3-16 (paragraph 0016)) and a dielectric gate structure (element 20 of FIGS. 2a-2d; page 5 lines 3-16 (paragraph 0016)). The method also includes forming lightly-doped extension regions in the semiconductor substrate adjacent each gate

stack (element 100 of FIGS. 2b-2d, page 5 line 16 through page 6 line 11 (paragraphs 0017-0019)), the lightly-doped extension regions in the N-type dopant region comprising a P-type dopant having a dopant concentration in the range of about 1-2 e20 atoms/cm3, forming a layer of silicon oxide (element 110 of FIGS. 2c-2d; page 6 line 11 through page 7 line 16 (paragraphs 0020-0024)) in contact with a total exposed surface of the lightly-doped extension regions (FIGS. 2c-2d; page 6 line 11 through page 7 line 16, page 9 lines 20-28 (paragraphs 0020-0024 and 0033)), and forming an interfacial layer of nitrogen (element 112 of FIGS. 2c-2d; page 6 line 11 through page 7 line 16 (paragraphs 0020-0024)) within the total exposed surface of the lighted-doped extension regions (page 6 lines 11-20 (paragraph 0020)) where the interfacial layer of nitrogen has an atomic nitrogen concentration in the range of 2-15 atomic percent (page 6 lines 11-20 (paragraph 0020)). In addition, the method includes forming at least one sidewall layer coupled to the layer of insulating material (page 7 line 16 through page 8 line 5 (paragraphs 0025-0026)), forming source and drain regions (element 140 of FIG. 2d; page 8 lines 5-11 (paragraph 0027)) in the semiconductor substrate adjacent to each of the gate stacks where the source and drain regions in the N-type dopant region comprise a P-type dopant having a concentration in the range of about 1-2 e20 atoms/cm3. Furthermore, the method includes forming a capping layer (element 132 of FIG. 2d; page 8 line 11 through page 9 line 20 (paragraph 0028-0032)) of contiguous silicon nitride having a thickness in the range of about 200-1000 angstroms (page 8 lines 11-18

(paragraph 0028)). Moreover, the method includes annealing (page 8 lines 18-23 (paragraph 0029)), after the formation of the capping layer and with the capping layer in place, the extension regions and the source and drain regions at a temperature in the range of 1000-1100 degrees centigrade for a period in the range of less than about 10 seconds (page 8 lines 18-23 (paragraph 0029)), and removing all of the nitride cap after the annealing (page 8 lines 23-28 (paragraph 0030)).

Claim 19 is dependant on Claim 1 and further specifies that the steps of forming the layer of insulating material and forming the interfacial layer of nitrogen are performed without breaking vacuum (page 7 lines 6-12 (paragraph 0023)).

Claim 20 is dependant on Claim 10 and further specifies that the steps of forming the layer of insulating material and forming the interfacial layer of nitrogen are performed without breaking vacuum (page 7 lines 6-12 (paragraph 0023)).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1-10 and 19-20 stand rejected under 35 U.S.C. §103(a) as unpatentable over the patent publication of Wieczorek et al. (U.S. Pat. Pub. No. 2004/0061228 A1) in view of the patent publication of Chen et al. (U.S. Pat. Pub. No. 2005/0136583 A1).

ARGUMENT

Rejection of Claims 1-10 and 19-20 under 35 U.S.C. §103(a) as unpatentable over the patent publication of Wieczorek et al. (U.S. Pat. Pub. No. 2004/0061228 A1) in view of the patent publication of Chen et al. (U.S. Pat. Pub. No. 2005/0136583 A1).

Claim 1

Independent Claim 1 positively recites forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions, forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions, and forming at least one sidewall layer coupled to the layer of insulating material. These advantageously claimed features are neither taught nor suggested by the patent publications of Wieczorek et al. and Chen et al.

Wieczorek et al. does not teach the advantageously claimed invention because Wieczorek et al. does not teach forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions (FIGS. 1a and 2c; paragraphs 0012, 0039). In addition, Wieczorek et al. does not teach

forming at least one sidewall layer coupled to the layer of insulating material (paragraphs 0008, 0032, 0036, 0044; FIGS. 1a-2e).

The Appellants respectfully traverse the statements in the Office Action (page 4) that the layer of insulating material is element 209 (in FIG. 2d) of Wieczorek et al. The Appellants submit that the layer of insulating material and the sidewall layer (coupled to the layer of insulating material) are advantageously claimed as two separate elements; therefore, element 209 of Wieczorek et al. cannot anticipate both positively recited elements of the Appellants' independent Claim 1 (the Appellants note that the Office Action does not list any element or teaching of Wieczorek et al. for the advantageously claimed sidewall layer (page 4)).

Chen et al. does not teach the advantageously claimed invention because Chen et al. does not teach forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions (FIGS. 3-5 and 7; paragraphs 0034, 0062). In addition, Chen et al. does not teach forming at least one sidewall layer coupled to the layer of insulating material (paragraph 0028; FIGS. 1-7).

Because neither Wieczorek et al. nor Chen et al. teach the step of forming a layer of insulating material in contact with a total exposed surface of the lightly-

doped extension regions; the combination of Wieczorek et al. and Chen et al. does not teach the advantageously claimed step of forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions. Similarly, neither Wieczorek et al. nor Chen et al. teach the step of forming at least one sidewall layer coupled to the layer of insulating material; therefore, the combination of Wieczorek et al. and Chen et al. also does not teach the advantageously claimed step of forming at least one sidewall layer coupled to the layer of insulating material.

Therefore, Claim 1 is patentable over the patent publications of Wieczorek et al. and Chen et al.

Claim 2

Claim 2 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 2 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitations of Claim 1, are neither taught nor suggested by the patent publications of Wieczorek et al. and Chen et al. Namely, Claim 2 further specifies the additional limitation that the extension regions for the PMOS transistors have a dopant concentration in the range of about 1-2 e20 atoms/cm3.

The Appellants respectfully traverse the assertion (on page 6 of the Office Action) that Wieczorek et al. teaches the dopant concentration of the extension regions in paragraph 0034. The Appellants submit that paragraph 0034 of Wieczorek et al. is directed to the concentration of the barrier diffusion material; however, the barrier diffusion is a different element than the extension regions (note that the extension regions do not exist at the manufacturing step described in paragraph 0034 (corresponding to FIG. 2b) – rather, the extension regions are formed in paragraph 0037 (element 205 of FIG. 2c)).

Because neither Wieczorek et al. nor Chen et al. teach the step of forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions - as required by the combination of Claims 1 and 2 - the combination of Wieczorek et al. and Chen et al. also does not teach the advantageously claimed step of forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions. Similarly, neither Wieczorek et al. nor Chen et al. teach the step of forming at least one sidewall layer coupled to the layer of insulating material - as required by the combination of Claims 1 and 2 - therefore, the combination of Wieczorek et al. and Chen et al. also does not teach the advantageously claimed step of forming at least one sidewall layer coupled to the layer of insulating material.

Therefore, Claim 2 is patentable over the patent publications of Wieczorek et al. and Chen et al.

Claim 3

Claim 3 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 3 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitations of Claim 1, are neither taught nor suggested by the patent publications of Wieczorek et al. and Chen et al. Namely, Claim 3 further specifies the additional limitation that the source and drain regions for the PMOS transistors have a dopant concentration in the range of about 1-2 e20 atoms/cm3.

The Appellants respectfully traverse the assertion (on page 6 of the Office Action) that Wieczorek et al. teaches the dopant concentration of the source and drain regions in paragraph 0034. The Appellants submit that paragraph 0034 of Wieczorek et al. is directed to the concentration of the barrier diffusion material; however, the barrier diffusion is a different element than the source and drain regions (note that the source and drain regions do not exist at the manufacturing step described in paragraph 0034 (corresponding to FIG. 2b) – rather, the source and drain regions are formed in paragraph 0037 (element 204 of FIG. 2c)).

Because neither Wieczorek et al. nor Chen et al. teach the step of forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions - as required by the combination of Claims 1 and 3 - the combination of Wieczorek et al. and Chen et al. also does not teach the advantageously claimed step of forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions. Similarly, neither Wieczorek et al. nor Chen et al. teach the step of forming at least one sidewall layer coupled to the layer of insulating material - as required by the combination of Claims 1 and 3 - therefore, the combination of Wieczorek et al. and Chen et al. also does not teach the advantageously claimed step of forming at least one sidewall layer coupled to the layer of insulating material.

Therefore, Claim 3 is patentable over the patent publications of Wieczorek et al. and Chen et al.

Claim 4

Claim 4 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 4 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitations of Claim 1, are neither taught nor suggested by the patent publications of Wieczorek et al. and Chen et al. Namely, Claim 4 further specifies

the additional limitation that the interfacial nitride layer has an atomic nitrogen concentration in the range of 2-15 atomic percent.

The Appellants respectfully traverse the assertion (on page 6 of the Office Action) that Wieczorek et al. teaches the atomic nitrogen concentration of the interfacial nitride layer in paragraph 0034. Chen et al. also does not teach an atomic nitrogen concentration of an interfacial nitride layer (paragraph 0012). Therefore, the combination of Wieczorek et al. and Chen et al. also does not teach the advantageously claimed atomic nitrogen concentration of an interfacial nitride layer in the range of 2-15 atomic percent.

Therefore, Claim 4 is patentable over the patent publications of Wieczorek et al. and Chen et al.

Claim 5

Claim 5 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 5 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitations of Claim 1, are neither taught nor suggested by the patent publications of Wieczorek et al. and Chen et al. Namely, Claim 5 further specifies

the additional limitation that the insulting layer is selected from the group comprising silicon nitride and silicon oxide.

The Appellants respectfully traverse the assertion (on page 6 of the Office Action) that Wieczorek et al. teaches the composition of the insulating layer in paragraphs 0032-0033. The Appellants submit that paragraphs 0032-0033 of Wieczorek et al. teach the composition of the sidewall spacers 220 that are a separately claimed element from the insulating layer (similarly, paragraph 0033 of Wieczorek et al. teaches the composition of the gate insulation layer 207 that is a separately claimed element from the insulating layer). Chen et al. also does not teach the composition of an insulating layer (paragraph 0062). Therefore, the combination of Wieczorek et al. and Chen et al. also does not teach the advantageously claimed insulting layer selected from the group comprising silicon nitride and silicon oxide.

Therefore, Claim 5 is patentable over the patent publications of Wieczorek et al. and Chen et al.

Claim 6

Claim 6 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 6 is allowable on its own

merits because it recites additional features of the invention that, in combination with the limitations of Claim 1, are neither taught nor suggested by the patent publications of Wieczorek et al. and Chen et al. Namely, Claim 6 further specifies the additional limitation that the step of forming an interfacial layer of nitrogen is performed using one of the methods selected from the group comprising an NH_3 thermal annealing, an NH_3 or N_2 plasma treatment, or an N implantation.

The Appellants submit that neither Wieczorek et al. (paragraph 0034) nor Chen et al. (0062) teach forming an interfacial layer of nitrogen with a NH_3 thermal anneal. Moreover, neither Wieczorek et al. nor Chen et al. teach the step of forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions - as required by the combination of Claims 1 and 6 – therefore, the combination of Wieczorek et al. and Chen et al. also does not teach the advantageously claimed step of forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions. Similarly, neither Wieczorek et al. nor Chen et al. teach the step of forming at least one sidewall layer coupled to the layer of insulating material - as required by the combination of Claims 1 and 6 - therefore, the combination of Wieczorek et al. and Chen et al. also does not teach the advantageously claimed step of forming at least one sidewall layer coupled to the layer of insulating material.

Therefore, Claim 6 is patentable over the patent publications of Wieczorek et al. and Chen et al.

Claim 7

Claim 7 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 7 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitations of Claim 1, are neither taught nor suggested by the patent publications of Wieczorek et al. and Chen et al. Namely, Claim 7 further specifies the additional limitation that the capping layer has a thickness in the range of 200-1000 angstroms.

Neither Wieczorek et al. nor Chen et al. teach the step of forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions - as required by the combination of Claims 1 and 7 – therefore, the combination of Wieczorek et al. and Chen et al. also does not teach the advantageously claimed step of forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions. Similarly, neither Wieczorek et al. nor Chen et al. teach the step of forming at least one sidewall layer coupled to the layer of insulating material - as required by the combination of Claims 1 and 7 - therefore, the combination of Wieczorek et al.

and Chen et al. also does not teach the advantageously claimed step of forming at least one sidewall layer coupled to the layer of insulating material.

Therefore, Claim 7 is patentable over the patent publications of Wieczorek et al. and Chen et al.

Claim 8

Claim 8 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 8 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitations of Claim 1, are neither taught nor suggested by the patent publications of Wieczorek et al. and Chen et al. Namely, Claim 8 further specifies the additional limitation that the annealing step is performed in the range of 1000-1100 degrees centigrade for a time in the range of less than about 10 seconds.

Neither Wieczorek et al. nor Chen et al. teach the step of forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions - as required by the combination of Claims 1 and 8 – therefore, the combination of Wieczorek et al. and Chen et al. also does not teach the advantageously claimed step of forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions. Similarly,

neither Wieczorek et al. nor Chen et al. teach the step of forming at least one sidewall layer coupled to the layer of insulating material - as required by the combination of Claims 1 and 8 - therefore, the combination of Wieczorek et al. and Chen et al. also does not teach the advantageously claimed step of forming at least one sidewall layer coupled to the layer of insulating material.

Therefore, Claim 8 is patentable over the patent publications of Wieczorek et al. and Chen et al.

Claim 9

Claim 9 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 9 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitations of Claim 1, are neither taught nor suggested by the patent publications of Wieczorek et al. and Chen et al. Namely, Claim 9 further specifies the additional limitation that the step of forming at least one sidewall layer includes the use of a BTBAS precursor.

The Appellants respectfully traverse the assertion (on page 7 of the Office Action) that Chen et al. teaches the precursor used in the step of forming a sidewall layer in paragraph 0046. The Appellants submit that paragraph 0046 of

Chen et al. is directed to the precursor used during the formation of the capping layer 24 (see paragraph 0042) that is a different element from the sidewall spacer 16.

Because neither Wieczorek et al. nor Chen et al. teach the step of forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions - as required by the combination of Claims 1 and 9 - the combination of Wieczorek et al. and Chen et al. also does not teach the advantageously claimed step of forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions. Similarly, neither Wieczorek et al. nor Chen et al. teach the step of forming at least one sidewall layer coupled to the layer of insulating material - as required by the combination of Claims 1 and 9 - therefore, the combination of Wieczorek et al. and Chen et al. also does not teach the advantageously claimed step of forming at least one sidewall layer coupled to the layer of insulating material.

Therefore, Claim 9 is patentable over the patent publications of Wieczorek et al. and Chen et al.

Claim 10

Independent Claim 10 positively recites forming a layer of silicon oxide in contact with a total exposed surface of the lightly-doped extension regions, forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions, and forming at least one sidewall layer coupled to the layer of insulating material. These advantageously claimed features are neither taught nor suggested by the patent publications of Wieczorek et al. and Chen et al.

Wieczorek et al. does not teach the advantageously claimed invention because Wieczorek et al. does not teach forming a layer of silicon oxide in contact with a total exposed surface of the lightly-doped extension regions (FIGS. 1a and 2c; paragraphs 0012, 0039). In addition, Wieczorek et al. does not teach forming at least one sidewall layer coupled to the layer of insulating material (paragraphs 0008, 0032, 0036, 0044; FIGS. 1a-2e).

The Appellants respectfully traverse the statements in the Office Action (page 8) that Wieczorek et al. teaches the formation of a layer of silicon oxide in contact with a total exposed surface of the lightly-doped extension regions in paragraphs 0033-0034. The Appellants submit that the layer of silicon oxide and the sidewall layer are advantageously claimed as two separate elements; therefore,

element 220 of Wieczorek et al. cannot anticipate both positively recited elements of the Appellants' independent Claim 10 (the Appellants note that the cited paragraph 0034 of Wieczorek et al. does not discuss any dielectric element).

Chen et al. does not teach the advantageously claimed invention because Chen et al. does not teach forming a layer of silicon oxide in contact with a total exposed surface of the lightly-doped extension regions (FIGS. 3-5 and 7; paragraphs 0034, 0062). In addition, Chen et al. does not teach forming at least one sidewall layer coupled to the layer of insulating material (paragraph 0028; FIGS. 1-7).

Because neither Wieczorek et al. nor Chen et al. teach the step of forming a layer of silicon oxide in contact with a total exposed surface of the lightly-doped extension regions; the combination of Wieczorek et al. and Chen et al. does not teach the advantageously claimed step of forming a layer of silicon oxide in contact with a total exposed surface of the lightly-doped extension regions. Similarly, neither Wieczorek et al. nor Chen et al. teach the step of forming at least one sidewall layer coupled to the layer of insulating material; therefore, the combination of Wieczorek et al. and Chen et al. also does not teach the advantageously claimed step of forming at least one sidewall layer coupled to the layer of insulating material.

Therefore, Claim 10 is patentable over the patent publications of Wieczorek et al. and Chen et al.

Claim 19

Claim 19 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 19 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitations of Claim 1, are neither taught nor suggested by the patent publications of Wieczorek et al. and Chen et al. Namely, Claim 19 further specifies the additional limitation that the steps of forming the layer of insulating material and forming the interfacial layer of nitrogen are performed without breaking vacuum.

The Appellants respectfully traverse the assertion (on page 10 of the Office Action) that when the cited references fail to teach an advantageously claimed step that "the process is understood to be performed". The Appellants respectfully submit the Examiner has failed to establish a prima facie case of obviousness. (*Ex parte* Humphreys, 24 USPQ2d 1255, 1262.)

Wieczorek et al. does not teach forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions plus

forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions (paragraphs 0032-0036; FIGS. 2a-2c); therefore, Wieczorek et al. cannot teach that the steps of forming the layer of insulating material and forming the interfacial layer of nitrogen are performed without breaking vacuum, as advantageously claimed. Similarly, Chen et al. does not teach forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions plus forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions (paragraphs 0024-0034; FIGS. 1-3); therefore, Chen et al. cannot teach that the steps of forming the layer of insulating material and forming the interfacial layer of nitrogen are performed without breaking vacuum, as advantageously claimed. Because neither Wieczorek et al. nor Chen et al. teach that the steps of forming the layer of insulating material and forming the interfacial layer of nitrogen are performed without breaking vacuum; the combination of Wieczorek et al. and Chen et al. also does not teach the advantageously claimed steps of forming the layer of insulating material and forming the interfacial layer of nitrogen are performed without breaking vacuum.

Therefore, Claim 19 is patentable over the patent publications of Wieczorek et al. and Chen et al.

Claim 20

Claim 20 is dependent on Claim 10 and is therefore allowable for the same reasons that Claim 10 is allowable. Furthermore, Claim 20 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitations of Claim 10, are neither taught nor suggested by the patent publications of Wieczorek et al. and Chen et al. Namely, Claim 20 further specifies the additional limitation that the steps of forming the layer of silicon oxide and forming the interfacial layer of nitrogen are performed without breaking vacuum.

The Appellants respectfully traverse the assertion (on page 10 of the Office Action) that when the cited references fail to teach an advantageously claimed step that "the process is understood to be performed". The Appellants respectfully submit the Examiner has failed to establish a prima facie case of obviousness. (*Ex parte* Humphreys, 24 USPQ2d 1255, 1262.)

Wieczorek et al. does not teach forming a layer of silicon oxide in contact with a total exposed surface of the lightly-doped extension regions plus forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions (paragraphs 0032-0036; FIGS. 2a-2c); therefore, Wieczorek et al. cannot teach that the steps of forming the layer of silicon oxide

and forming the interfacial layer of nitrogen are performed without breaking vacuum, as advantageously claimed. Similarly, Chen et al. does not teach forming a layer of silicon oxide in contact with a total exposed surface of the lightly-doped extension regions plus forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions (paragraphs 0024-0034; FIGS. 1-3); therefore, Chen et al. cannot teach that the steps of forming the layer of silicon oxide and forming the interfacial layer of nitrogen are performed without breaking vacuum, as advantageously claimed. Because neither Wieczorek et al. nor Chen et al. teach that the steps of forming the layer of silicon oxide and forming the interfacial layer of nitrogen are performed without breaking vacuum; the combination of Wieczorek et al. and Chen et al. also does not teach the advantageously claimed steps of forming the layer of silicon oxide and forming the interfacial layer of nitrogen are performed without breaking vacuum.

Therefore, Claim 20 is patentable over the patent publications of Wieczorek et al. and Chen et al.

CONCLUSION

For the reasons stated above, the Appellants respectfully contend that each claim is patentable. Therefore, the reversal of all rejections is courteously solicited.

Respectfully submitted,

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CLAIMS APPENDIX

1. A method for fabricating a CMOS transistor structure, comprising the steps of:

providing a semiconductor substrate having a P-type dopant region to support an N-channel transistor of the CMOS transistor structure and an N-type dopant region to support a P-channel transistor of the CMOS transistor structure, each of the N-type dopant and P-type dopant regions having an overlying gate stack including a conductive gate structure and a dielectric gate structure;

forming lightly-doped extension regions in the semiconductor substrate adjacent each gate stack;

forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions;

forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions;

forming at least one sidewall layer coupled to the layer of insulating material;

forming source and drain regions in the semiconductor substrate adjacent to each of the gate stacks;

forming a capping layer of contiguous silicon nitride over the semiconductor substrate;

annealing, after the formation of the capping layer and with the capping

layer in place, the extension regions and the source and drain regions; and

removing all of the capping layer after the annealing.

2. The method of claim 1 wherein the extension regions for the PMOS transistors have a dopant concentration in the range of about 1-2 e20 atoms/cm3.

3. The method of claim 1 wherein the source and drain regions for the PMOS transistors have a dopant concentration in the range of about 1-2 e20 atoms/cm3.

4. The method of claim 1 wherein said interfacial nitride layer has an atomic nitrogen concentration in the range of 2-15 atomic percent.

5. The method of claim 1 wherein the insulting layer is selected from the group comprising silicon nitride and silicon oxide.

6. The method of claim 1 wherein the step of forming an interfacial layer of nitrogen is performed using one of the methods selected from the group comprising an NH_3 thermal annealing, an NH_3 or N_2 plasma treatment, or an N implantation.

7. The method of claim 1 wherein the capping layer has a thickness in the range of 200-1000 angstroms.

8. The method of claim 1 wherein the annealing step is performed in the range of 1000-1100 degrees centigrade for a time in the range of less than about 10 seconds.

9. The method of claim 1 wherein the step of forming at least one sidewall layer includes the use of a BTBAS precursor.

10. A method for fabricating a CMOS transistor structure, comprising the steps of:

providing a semiconductor substrate having an N-type dopant region to support an PMOS transistor of the CMOS transistor structure and a P-type dopant region to support a NMOS transistor of the CMOS transistor structure, each of the N-type dopant and P-type dopant regions having an overlying gate stack including a conductive gate structure and a dielectric gate structure;

forming lightly-doped extension regions in the semiconductor substrate adjacent each gate stack, the lightly-doped extension regions in the N-type dopant region comprising a P-type dopant having a dopant concentration in the range of about 1-2 e20 atoms/cm3;

forming a layer of silicon oxide in contact with a total exposed surface of

the lightly-doped extension regions;

forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions, the interfacial layer of nitrogen having an atomic nitrogen concentration in the range of 2-15 atomic percent;

forming at least one sidewall layer coupled to the layer of insulating material;

forming source and drain regions in the semiconductor substrate adjacent to each of the gate stacks, the source and drain regions in the in the N-type dopant region comprising a P-type dopant having a concentration in the range of about 1-2 e20 atoms/cm3;

forming a capping layer of contiguous silicon nitride having a thickness in the range of about 200-1000 angstroms over the semiconductor substrate;

annealing, after the formation of the capping layer and with the capping layer in place, the extension regions and the source and drain regions at a temperature in the range of 1000-1100 degrees centigrade for a period in the range of less than about 10 seconds; and

removing all of the nitride cap after the annealing.

19. The method of claim 1 wherein the steps of forming the layer of insulating material and forming the interfacial layer of nitrogen are performed without breaking vacuum.

20. The method of claim 10 wherein the steps of forming the layer of silicon oxide and forming the interfacial layer of nitrogen are performed without breaking vacuum.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None